

Dolphin PCI Express PXH832 Adapter



PXH832 Transparent Adapter Users Guide Version 1.21

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PCI Express External Cabling specification 3.0 is as of the release of MXH832 not completed and ratified by the PCI-SIG. The MXH832 is designed to the new specification, but Dolphin cannot guarantee the card will be compliant to the final 1.0 version. Dolphin firmware tools can update the CMI implementation. Do not use information in this guide to design your own card, always reference the original PCI SIG External Cabling Specification for details.

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ENVIRONMENTAL POLICY

Dolphin is minimizing the amount of printed documentation and software CDs in its shipments; please download additional documentation and software from www.dolphinics.com.

Terms and Acronyms

Important terms and acronyms used in this manual

AOC	Active Optical Cable. PCIe fiber cable assembly.
CMI	Cable M anagement Interface. The 2-wire management interface for communication between subsystems connected by a PCIe 3.0 cable. Details can be found in the PCI-SIG External Cabling Specification 3.0.
ВМС	Microcontroller on the PXH832 used to manage and implement the CMI communications and other board management functions.
eXpressWare	Dolphin's software stack for PCIe clustering and IO. Please visit <u>http://www.dolphinics.com/software</u> for more information.
Lane	One PCI Express Lane contains a differential pair for transmission and a differential pair for reception.
Link	A collection of one or more PCI Express Lanes providing the communication path between an Upstream and Downstream Port.
MiniSAS-HD	Standard cable without CMI support. SFF-8644 connectors.
PCIe 3.0 cable	PCIe cable compliant to the new PCI-SIG External Cabling Specification 3.0. Support for CMI. SFF-8644 connectors.
Port	The PXH832 has four x4 ports, named P1, P2, P3, P4. The physical ports are identified by text on the PCIe brackets.
Wake	A mechanism used by a downstream device to request the reapplication of main power when in the L2 Link state.

PXH832 High Level Specification

The PXH832 is a low profile, half-length PCIe adapter that can be configured as a Transparent Host Adapter card or a Target adapter card. Once installed in any server's or PC's PCI Express compliant slot, a PXH832 can connect to another PXH832 configured for Transparent Target operation or any target device compliant to the PCI Express External Cabling Specification 3.0. The PXH832 configured as a Transparent Target card can be installed in a PCI Express compliant expansion upstream slot. Please contact Dolphin for a list of compliant expansion chassis. The PXH832 supports PCIe Gen1, Gen2 and Gen3 speeds and x1, x2, x4, x8 and x16 link-widths. The card will operate at the highest common speed shared between the slot and the card (Gen3) and the widest common link-width (x16).

- PCI Express Base Specification, Rev. 3.0.
- PCI Express CEM Specification, Rev. 3.0.
- PCI Express External Cabling specification 3.0 (Work in progress, rev 0.9)
- PCI Express Gen3 8.0 GT/s per lane signaling 128 GT/s total signaling.
- PCI Express Gen3 x16 edge connector. The card installs in any PCI Express slot that has a physical x16 connector.
- Compliant with PCI Express Gen1 through Gen3 computers and IO systems, auto detection.
- The PXH832 supports transparent connections to IO systems (Host and Target operation).
- Quad SFF-8644 cable connector
 - Durability max total 250 mating cycles
- Cable port configurations, up to
 - o One x16
 - o Two x8
 - o Four x4
- Broadcom / Avago / PLX PEX8733 PCI Express Gen3 chipset.
- 132 nanosecond cut-through latency port to port.
- Support for MiniSAS-HD copper cables up to 9 meters (between PXH832 cards).
- Support for PCI Express 3.0 copper cables with CMI.
- Support for active optical fibers up to 100 meters.
- Low profile, Half length PCI Express Electromechanical Specification, Rev 2.0.
- Dimensions 167.65mm (6.600 inches) x 68.90 mm (2.731 inches)
- Comes with both low profile and standard profile PCI Express bracket.
- Host clock isolation. Automatic support for host running CFC or SSC mode.
- VAUX powered board management controllers for flexible configuration and cable management.
- EEPROM recovery option.
- No PCI Express power domain isolation.
- Power consumption:
 - 12 Volt: Max 14 Watt, typical 10 Watts without AOC attached.
 - +3.3 Volt: Max 3.3 Watt
 - +3.3 Volt AUX: Max 1 Watt
- Port power supply (per cable port): 3.3 Volt +/- 5%, 0.6 A
- Operating Temperature: 0°C 55°C (32°F 131°F), Air Flow: 150 LFM
- Operating Temperature with AOC: 0°C 45°C (32°F 113°F), Air Flow: 150 LFM
- Operating Temperature: 0°C 50°C (32°F 122°F), Air Flow: ~0 LFM
- Relative Humidity: 5% 95% (non- condensing)
 - Regulatory
 - o CE
 - o Compliant to EN-55022 (2010), EN 55024 (2010), EN 61000-6-2 (2005), Class A.
 - o RoHS
 - FCC Class A.
 - o WEEE

MTBF by Temperature and Environment

The MTBF (in hours) for the PXH832 can be found in the table below. The numbers are calculated using the Telcordia SR-332 issue 2 (2006) standard.

Ambient	Environment			
Temp [°C]	Ground fixed, controlled	Ground fixed, uncontrolled	Ground mobile	
0	6.054.808	3.027.404	1.009.135	
5	5.125.130	2.562.565	854.188	
10	4.307.782	2.153.891	717.964	
15	3.598.507	1.799.254	599.751	
20	2.990.475	1.495.238	498.413	
25	2.474.892	1.237.446	412.482	
30	2.041.816	1.020.908	340.303	
35	1.680.915	840.458	280.153	
40	1.382.069	691.034	230.345	
45	1.135.823	567.911	189.304	
50	933.648	466.824	155.608	
55	768.059	384.030	128.010	

Table 1: MTBF vs. Temperature and Environment

Packaging

The PXH832 includes the following components.

- PXH832 Adapter Board
- Low profile bracket
- Anti-static bag
- Getting started guide

Pre-Installation Questions

Certain steps should be taken prior to installing the PXH832. You should determine the following configuration requirements.

- Which PCIe slot and system will the card be installed in?
- Will the board act as a host adapter or target adapter?
- What is the speed and link width of the slot that the card will be installed in?
- What is the operating environment in which the card will be installed?
- What type and length of cables will be used?
- How to establish proper operational conditions, temperature and airflow.

PCIe Slot Determination

The PXH832 supports PCIe Gen1, Gen2 and Gen3 speeds and x1, x2, x4, x8 and x16 link-widths. The slot width and speed will affect the performance of the card. The card can be physically installed in a x4, x8 or x16 connector. The card will auto configure to the slot speed and width.

PXH832 Host / Target Configuration

The PXH832 can act as either a host adapter or target adapter. The PXH832 has a DIP switch bank to control these functions. The DIP switch labeled SW1 can be found close to the upper edge of the board. The main configuration options are host or target operations. The default DIP switch setting is transparent host x16 operations. Additional settings are target operations, two x8 links, four x4 links or tuning for long copper cables.

Operating Environment

To maximize lifetime for the product and maintain the warranty, please honor the specified operating temperature and make sure the specified air flow is present. Special care should be considered when PXH832 is used in office type cabinets in combination with other high energy consuming PCIe devices, e.g. not active cooled GPUs:

Operating Temperature: $0^{\circ}C - 55^{\circ}C (32^{\circ}F - 131^{\circ}F)$, Air Flow: 150 LFM Operating Temperature with AOC: $0^{\circ}C - 45^{\circ}C (32^{\circ}F - 113^{\circ}F)$, Air Flow: 150 LFM Operating Temperature: $0^{\circ}C - 50^{\circ}C (32^{\circ}F - 122^{\circ}F)$, Air Flow: ~0 LFM

Cable Connections

The PXH832 is designed to support both long and short copper cables and comes with two types of PCIe link tuning parameters. The default configuration supports copper cables between 0.5 and 3 meters or fiber cables (AOC). To use copper cables longer than 3 meters, please use DIP-Switch OPT2 to enable the long cable tuning. If you are connecting the PXH832 to a compliant target device not designed by Dolphin, other settings or limitations may apply.

The PXH832 cable connector is compliant to the SFF-8644 industry specification and supports standard x4/x8 Mini-SAS HD cables or x4/x8 PCI Express 3.0 cables compliant to the PCIe External Cabling Specification 3.0. Four x4 or two x8 cables are needed for full PCIe x16 connectivity.

Cable ports

The PXH832 has a quad SFF-8644 connector. Each port implements 4 PCIe lanes. The ports are numbered as shown in Figure 1 PCIe bracket below.

PCI Express 3.0 cables

When used with cables compliant to the new PCIe External Cable standard 3.0, the PXH832 card will transmit a CMI Reset message downstream. The card can be connected to a PXH832 in Target mode or any PCIe device compliant to the new cable standard.

MiniSAS-HD cables

When used with standard MiniSAS-HD cables that does not support the new CMI functionality, the onboard CPU will synthetize a PCIe #CPERST and forward it to the downstream PXH832 card. CWAKE and CPOWERON is not supported using standard MiniSAS-HD cables.

Active Optical Cables (AOC)

The PXH832 card is compliant with active fiber optic PCIe cables up to 100 meters. No special configuration of the card needs to be performed for working with fibers. CWAKE and CPOWERON is not supported using standard AOC cables.

Please note: Only PCIe fiber cables available from Dolphin are supported. Standard MiniSAS-HD AOC cables are not supported.

CMI Functionality

The BMC version 8.12 firmware release and newer supports the following CMI operations:

- Publishes card and CMI status information in readable memory map
- Supports sending and receiving CMI reset, wake and power status messages
- Supports receiving indicators (LED/messages).

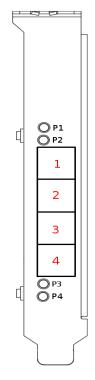


Figure 1 PCIe bracket

Installation

Step 1 - Unpack board

The PXH832 card is shipped in an anti-static bag to prevent static electricity damage. The card should only be removed from



the bag after ensuring that anti-static precautions are taken. Static electricity from your clothes or work environment can damage your PCI Express adapter card or your PC. Always wear a grounded anti-static wrist strap while opening the PC and when the PXH832 is removed from the anti-static bag. Unpack the PXH832 from the anti-static bag using proper anti-static procedures.

Step 2 - Change PCIe Bracket if necessary

The PXH832 package includes a standard and low-profile PCI Express bracket. By default, the standard height bracket is installed on the board. If you need to replace the mounted bracket with a low-profile bracket, carefully unscrew the two mounting screws to remove the full height bracket. Save the two mounting screws and replace the bracket with the low-profile bracket. Use the two mounting screws to install the low-profile bracket. The screws should be carefully tightened but be careful not to overtighten. Make sure you are properly grounded to avoid static discharges that may destroy the adapter card before performing this procedure.

Step 3 - Configure the Board for Proper Operation

Please note that this DIP switch setting below requires firmware 8.3 or newer. This is included with all PXH832 boards shipping form Dolphin 11th December 2017 or later. Users of older firmware should either upgrade the firmware or use an older users guide (version prior to 1.13).

The PXH832 has one bank of 8 DIP switches. The default factory setting for the PXH832 is Transparent mode, short cable, single (up to x16) link connection.

The PXH832 has DIP switches for setting special modes or operations. Please carefully read the documentation before modifying any DIP switch settings. Please pay close attention to ON and OFF positions written on the DIP switch.

DIP Switch Bank – Configuration



Figure 2: DIP Switch shows the DIP switch for the PXH832. It is used to configure the adapter card. Please leave all undocumented DIP switches in the default position. Table 2: DIP Switch settings shows all the various DIP switch settings for the PXH832. Please refer to the next pages for details.

Figure 2: DIP Switch

DIP no.	Name	Description	ON	OFF	Default
1	TRANSP	Configuration selector, details next page Step 3 - Configure the Board for Proper Operation			ON
2	TARGET	Enable Target or Host operation.	Adapter is configured for transparent Target operations	Adapter is configured for transparent Host operations	OFF
3	OPT1	Configuration selector, details next page			OFF
4	OPT2	Enable long copper cable configuration. Please use same setting on both Host and Target	Support copper cables of 4m and longer	Supports copper cables of 0.4-3m length or fiber optic cables	OFF
5	OPT3	For future use			OFF
6	OPT4	CMI Disable	Will DISABLE CMI	CMI is supported if a PCIe 3.0 cable is installed	OFF
7	RES	Holds the management processors in reset	Board management is held in reset	Normal operation	OFF
8	SAFE	Enables the card to boot if the EEPROM has been corrupted	Safe EEPROM	Normal operation	OFF

Table 2: DIP Switch settings

Note: Some DIP switch configuration options may be changed in the future versions. Please always consult the latest user guide for details. This document covers firmware version 12.

DIP-Switch settings for Host operation

The following DIP-Switch settings should be considered when configuring the PXH832 for Transparent Host operation:

Configuration PXH832 Host	DIP ON	DIP switch view
Transparent Host One x16 port (Transp set /Shipping Default)	Transparent	
Transparent Host One x16 port Long copper cable tuning	Transparent OPT-2	
Transparent Host Two x8 ports	Transparent OPT-1	
Transparent Host Two x8 ports Long copper cable tuning	Transparent OPT-1 OPT-2	
Transparent Host Four x4 ports		
Transparent Host Four x4 ports Long copper cable tuning	OPT-2	
Transparent Host One x16 port DMA	OPT-1	
Transparent Host One x16 port DMA + Long copper cable tuning	OPT-1 OPT-2	

Table 3: PXH832 SW1 Host configuration settings

The transparent PXH832 DMA configuration setting will enable the onboard DMA engine. A special DMA driver is required to utilize this DMA function.

DIP-Switch settings for Target operation

The following DIP-Switch settings should be considered when configuring the PXH832 for Transparent Target operation:

Configuration PXH832 Target	DIP ON	DIP switch view
Transparent Target x16 port (port 1+2+3+4) x8 port (port 1+2) x4 port (port 1)	Transparent Target	
Transparent Target Long copper cable tuning x16 port (port 1+2+3+4) x8 port (port 1+2) x4 port (port 1)	Transparent Target OPT-2	

Table 4: PXH832 SW1 Target configuration settings

Step 4 - Install the Adapter Card

Before installing the adapter card, make sure you are properly grounded to avoid static discharges that may destroy your



computer or the adapter card. Ensure you are properly grounded before opening your computer or the antistatic bag containing the PXH832. Please follow your computer's or expansion chassis' manual on how to install a PCI Express card.

The PXH832 Adapter card can be installed into any PCI Express x16 slot. The PXH832 supports PCI Express Gen1, Gen2 and Gen3 signaling. NOTE: A Gen3 slot is recommended as it typically doubles the performance

compared to a Gen2 slot. The PXH832 is an x16 card, so maximum performance will only be attained if the slot provides full electrical x16 signaling.

The PXH832 supports hosts using either spread spectrum or constant frequency clocking. The card implements clock isolation.

Step 5 - Installing and Removing the Cable

Installing and removing cables should be done with both host and expansion system powered off. Please contact your Dolphin representative if you intend to continuously connect and disconnect the PCI Express cables.

Connecting the Cable

Please carefully install the cable connector into the connector housing on the PXH832 adapter card. To install the cable, match the cable house with the connector on the PXH832 adapter card. Use even pressure to insert the connector until it is secure. Adhere to ESD guidelines when installing the cables to ensure you don't damage the board. Computer cables should always use strain relief to protect the connected equipment from excessive force on the cable. This is especially important for cables between racks. Note that for wider than x4 connections, the same cable-ports (i.e. port 1 through 4) should be used on both host and target for each individual cable, to ensure that the cards properly link up as x8 or x16.

The PXH832 supports both copper and active optical cables (AOC). Specifications can be found in Table 5. The max distance may change when connecting to other PCIe products.

Cable	Speed	Distance
Copper MiniSAS-HD	Gen3	9 meters
Copper MiniSAS-HD	Gen1	12 meters
Copper PCIe 3.0 cable	Gen3	TBD
Fiber optic (AOC)	Gen3	100 meters

Table 5: Cable Specifications

Disconnecting the Cable

Please carefully pull the release tab to release the cable from the locking latches and gently pull the cable out of the connector guides.

Step 6 - Verify Installation & LEDs

The PXH832 comes with 4 bi-color LEDs which show the corresponding cable port status according to Table 6: LED below.

The LEDs are visible through cut-outs in the PCIe bracket on each side of the cable connector block.

LED color	Function
Off	No cable installed
Yellow	Cable installed, no link
Green	Cable installed, link gen 3
Green blinking	Cable installed, link gen 1/2

Table 6: LED behavior

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Use Cases Summary and Settings

Table 7: Use Case DIP switch settings below gives an overview of the various use cases, settings and limitations.

Use case	Description	Host DIP switch setting	Target DIP switch setting
A	One Host system having a PXH832 in Host mode connecting to one PXH832 in Target mode or a 3rd party expansion system.	Transparent ON OPT2 on for long copper cables	Single setting for all Target configurations except for long / short copper cable setting
В	One Host system having a PXH832 in Host mode connecting to two PXH832s in Target mode or two 3rd party expansion systems.	Transparent ON OPT1 on to enable two x8 links OPT2 on for long copper cables	Transparent ON Target ON OPT2 on if long copper cables
С	One Host system having a PXH832 in Host mode connecting to four PXH832s in Target mode or four 3rd party expansion systems.	All DIPs off. OPT2 on for long copper cables	are used All other off

Table 7: Use Case DIP switch settings

Use Cases

The PXH832 card may be used as both a Host card and a Target card. A Host and Target card can be used as a pair, or the Host card can be used with a compliant Target device. The supported use cases and the DIP switch settings are summarized in Table 7: Use Case DIP switch settings. **Please use the table to identify the correct DIP switch settings**.

Use Case A - 1 Host – Single Expansion Configuration

The Host system has a PXH832 adapter configured for Host operation and a direct x4, x8 or x16 link to a PXH832 configured for Target operation.

Connecting the cables for single expansion, x16 link

To establish an x16 link, a given port number should be connected to the same port number on the other card.

Always connect a cable from Port #x to Port #x

Host Card Port	Target Card Port
P1	P1
P2	P2
РЗ	РЗ
P4	P4

Table 8: Required x16 cabling

A failure connecting any of the cables will cause the link to re-train to x8 or x4.

Figure 3: Use Case A

Connecting the cables for single expansion, x8 link

To establish an x8 link, please select one of the alternatives below. Select alternative 1 or 2.

Alternatives	Host Card Port	Target Card Port	
1	P1	P1	
	P2	P2	
2	P3	P1	
	P4	P2	
Table 0. Alternative v9 cabling			

Table 9: Alternative x8 cabling

Connecting the cables for 2 Node Configurations, x4 link

To establish an x4 link when in dual port mode, please connect any port on the Host card to Port P1 or P4 on the Target card.

Use Case B – 1 Host - Dual Expansion Configuration

The host has a PXH832 adapter configured for Host operation and a direct x4 or x8 cable connection is used to connect two independent downstream target systems.

Connecting the cables for Single Node Dual expansion, x8 link

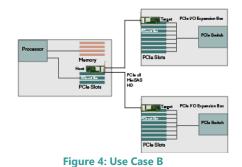
Connect the cables between the host and expansion as described above for x8 connectivity. Connect the second expansion to the free ports. Always connect to port P1 and P2 on the target card.

Use Case C – 1 Host - Quad Expansion Configuration

The host has a PXH832 adapter configured for Host mode and a direct x4 cable connection is used between the Host systems and each expansion Chassis. The PXH832 in the Expansion Chassis is configured for Target mode.

Connecting the cables for Single Node Four expansion, x4 link

Connect any port on the Host card to port P1 or P4 on the target card.



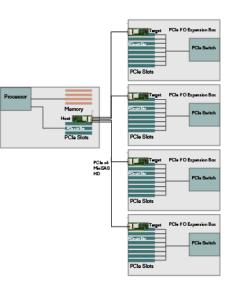


Figure 5: Use Case C

EEPROM and Firmware Upgrade

The PXH832 design uses a microcontroller (BMC) to implement the PCIe CMI protocol and other maintenance functions. Dolphin may from time to time publish updated firmware for the BMC firmware or EEPROM data for the card. Please note that standard PLX firmware tools cannot be used to upgrade the firmware. The current firmware version is 8.12. Please consult the PXH832 Firmware Release Note for details and instructions how to identify the firmware version and upgrade.

Identifying the Card

The card has a label-sticker with the serial number in the format 'PXH832-YY-ZZZZZZ', where YY denotes the card revision (e.g. CC) and ZZZZZZ denotes the serialized production number (e.g. 012345) – this whole string makes up the serial number of the card (i.e. PXH832-CC-012345).

You can also get this information using lspci in Linux:

First, identify the devices for the Dolphin Host card:

lspci l grep "Device 8733"

01:00.0 PCI bridge: PLX Technology, Inc. Device 8733 (rev ca) 02:08.0 PCI bridge: PLX Technology, Inc. Device 8733 (rev ca)

Then run lspci, and identify the card. It will show up as something like

lspci -s 1:0.0 -v
01:00.0 PCI bridge: PLX Technology, Inc. Device 8733 (rev ca) (prog-if 00 [Normal decode])
Flags: bus master, fast devsel, latency 0, IRQ 25
Memory at f7d00000 (32-bit, non-prefetchable) [size=256K]
Bus: primary=01, secondary=02, subordinate=03, sec-latency=0
Capabilities: [40] Power Management version 3
Capabilities: [48] MSI: Enable+ Count=1/8 Maskable+ 64bit+
Capabilities: [68] Express Upstream Port, MSI 00
Capabilities: [a4] Subsystem: Dolphin Interconnect Solutions AS Device 0832
Capabilities: [100] Device Serial Number 00-00-43-43-00-00-00-0a
Capabilities: [fb4] Advanced Error Reporting
Capabilities: [138] Power Budgeting
Capabilities: [10c] #19
Capabilities: [148] Virtual Channel
Capabilities: [e00] #12
Capabilities: [b00] Latency Tolerance Reporting
Capabilities: [b70] Vendor Specific Information: ID=0001 Rev=0 Len=010
Kernel driver in use: pcieport
Kernel modules: shpchp

Second, do

lspci -s 1:0.0 -v l grep -E "SubsystemlSerial" Capabilities: [a4] Subsystem: Dolphin Interconnect Solutions AS Device 0832 Capabilities: [100] Device Serial Number 00-00-43-43-00-00-00-0a

This shows the card as revision 0x4243 (hexadecimal values of the 'CC' letters in the ASCII table), with the production number 0x0000000A (0000010 in decimal).

Support

More information about the product, support and software download can be found at <u>http://www.dolphinics.com/px</u>. For general support questions, please contact Dolphin via the Jira Service Management portal: <u>https://www.dolphinics.com/csp</u>.

Technical Information

PCIe Cable Port Signals

The external PCI Express SFF-8644 cable connector supports the following signals:

- PETpN/PETnN: PCI Express Transmitter pairs, labeled where N is the Lane number (starting with 0); "p" is the true signal while "n" is the complement signal.
- PERpN/PERnN: PCI Express Receiver pairs, labeled where N is the Lane number (starting with 0); "p" is the true signal while "n" is the complement signal.
- PWR: Power to support AOC and signal conditioning components within the cable assembly.
- MGTPWR: Power supplied to the connector for cable management components that are needed while the link is not active. This needs to be active if the subsystem has power.
- CBLPRSNT#: Cable present detect, an active-low signal pulled-down by the cable when it is inserted into the PXH832 connector.
- CADDR: Signal used to configure the upstream cable management device address.
- CINT#: Signal asserted by the cable assembly to indicate a need for service via the CMI controller.
- CMISDA: Management interface data line. Used for both initial link setup and sideband messages when used with CMI compliant cables.
- CMISCL: Management interface clock line. Used for both initial link setup and sideband messages when used with CMI compliant cables.

				Column					
Row	9	8	7	6	5	4	3	2	1
D	GND	PETn2	PETp2	GND	PETn1	PETp1	GND	MGTPWR	PWR
С	GND	PETn3	PETp3	GND	PETn0	PETp0	GND	CMISDA	CMISCL
В	B GND PERn2 PERp2 GND PERn1 PERp1 GND CBLPRSNT# PWR								
А	GND	PERn3	PERp3	GND	PERn0	PERpO	GND	CINT#	CADDR
T 1 1 4	Table 10: Fotomral BCI and ashla Bin Out								

External PCIe x4 Cable Connector Pin-Out

Table 10; External PCIe x4 cable Pin-Out

PCIe Cable Port Mapping

The PXH832 card have a quad SFF-8644 connector. The ports are mapped as showed in the table below. The card utilized PCIe lane reversal.

Cable Port	x16	Dual x8	Quad x4	PCle 3.0 Cable Pin
	L15	L7	L3	TX0/RX0
1	L14	L6	L2	TX1/RX1
	L13	L5	L1	TX2/RX2
	L12	L4	LO	TX3/RX3
	L11	L3	L3	TX0/RX0
2	L10	L2	L2	TX1/RX1
2	L9	L1	L1	TX2/RX2
	L8	LO	LO	TX3/RX3
	L7	L7	L3	TX0/RX0
3	L6	L6	L2	TX1/RX1
5	L5	L5	L1	TX2/RX2
	L4	L4	LO	TX3/RX3
	L3	L3	L3	TX0/RX0
4	L2	L2	L2	TX1/RX1
4	L1	L1	L1	TX2/RX2
	LO	LO	LO	TX3/RX3

Table 11 : PCIe Cable Port Mapping

External PCIe x16 Edge Connector Pin-Out

The PXH832 Edge connector implements the signals found in the table below. Signals marked are bi-directional depending on if the card is configured for Transparent Host or Transparent Target.

1 +12 PRSNT1 2 +12 +12 3 +12 +12 4 GND GND 5 SMCLK BMC TCK JTAG - NC 6 SMDAT BMC TDI JTAG - NC 7 GND TDO JTAG - NC 9 TRST# JTAG - NC +3,3 PWR 10 +3,3V Standby +3,3 PWR 10 +3,3V Standby +3,3 PWR 11 WAKE# Wake up PERST# Reset 12 NC GND GND 11 13 GND Ref clock + Ref clock + 14 PERp0 GND I 16 15 PERn0 GND I 17 16 GND PETp0 I 17 17 PRSNT2# PETn0 I 18 18 GND GND I 19 20 PERp1 GND I 12 <	Pi	Side B	Descriptio	Side A	Descriptio
3 +12 +12 4 GND GND 5 SMCLK BMC TCK JTAG - NC 6 SMDAT BMC TDI JTAG - NC 7 GND TDO JTAG - NC 9 TRST# JTAG - NC +3,3 PWR 10 +3,3V Standby +3,3 PWR 10 +3,3V Standby +3,3 PWR 11 WAKE# Wake up PERST# Reset 12 NC GND	1	+12		PRSNT1	
4 GND GND 5 SMCLK BMC TCK JTAG - NC 6 SMDAT BMC TDI JTAG - TDI 7 GND TDO JTAG - NC 9 TRST# JTAG - NC +3,3 PWR 10 +3,3V Standby +3,3 PWR 10 +3,3V Standby +3,3 PWR 11 WAKE# Wake up PERST# Reset 12 NC GND GND GND 13 GND REFCLK Ref clock + 14 PERp0 GND GND 16 GND PETp0 IT 17 PRSNT2# PETn0 IT 18 GND GND IT 20 PERn1 GND IT 21 GND PETp1 IT 22 GND PETp2 IT 24 PERp2 GND IT	2	+12		+12	
5 SMCLK BMC TCK JTAG - NC 6 SMDAT BMC TDI JTAG - TDI 7 GND TDO JTAG - TDI 8 +3,3V PWR TMS JTAG - NC 9 TRST# JTAG - NC +3,3 PWR 10 +3,3V Standby +3,3 PWR 11 WAKE# Wake up PERST# Reset 12 NC GND 1 GND 13 GND REFCLK Ref clock + 14 PERp0 GND GND 16 GND PETp0 1 17 PRSNT2# PETn0 1 18 GND GND 1 19 PERp1 NC 2 20 PERn1 GND 1 21 GND PETp1 2 22 GND PETp2 2 23 GND PETp2 2 </td <td></td> <td>+12</td> <td></td> <td>+12</td> <td></td>		+12		+12	
6 SMDAT BMC TDI JTAG - 7 GND TDO JTAG - TDI 8 +3,3V PWR TMS JTAG - NC 9 TRST# JTAG - NC +3,3 PWR 10 +3,3V Standby +3,3 PWR 11 WAKE# Wake up PERST# Reset 12 NC GND 1 13 GND NC GND 1 14 PERp0 REFCLK Ref clock + 14 PERp0 GND 1 1 16 GND PETp0 1 1 17 PRSNT2# PETn0 1 1 18 GND GND 1 1 1 19 PERp1 NC 2 1 NC 20 PERn1 GND 1 1 1 1 21 GND PETp1 2 2 1 1 <td>4</td> <td>GND</td> <td></td> <td>GND</td> <td></td>	4	GND		GND	
7 GND TDO JTAG-TDI 8 +3,3V PWR TMS JTAG-NC 9 TRST# JTAG-NC +3,3 PWR 10 +3,3V Standby +3,3 PWR 11 WAKE# Wake up PERST# Reset 12 NC GND Image: additional system of the syste		SMCLK	вмс	ТСК	JTAG - NC
8 +3,3V PWR TMS JTAG -NC 9 TRST# JTAG - NC +3,3 PWR 10 +3,3V Standby +3,3 PWR 11 WAKE# Wake up PERST# Reset 12 NC GND Reset 12 NC GND Reset 12 NC GND Reset 13 GND REFCLK Ref clock + 14 PERp0 GND Ref clock - 15 PERn0 GND GND 16 GND PETp0 NC 17 PRSNT2# PETn0 NC 20 PERp1 NC ONC 21 GND PETp1 QU 22 GND PETp2 QU 24 PERp2 GND QU 25 GND PETp3 QU 26 GND PETp3 QU 29 GND	6	SMDAT	вмс	TDI	JTAG -
9 TRST# JTAG - NC +3,3 PWR 10 +3,3V Standby +3,3 PWR 11 WAKE# Wake up PERST# Reset 12 NC GND Reset 13 GND REFCLK Ref clock + 14 PERp0 GND Ref clock - 15 PERn0 GND GND Intersector 16 GND PETp0 NC 20 17 PRSNT2# PETn0 NC 20 20 PERp1 GND PETp1 22 21 GND PETp1 22 GND 24 23 PERp2 GND PETp2 26 GND 25 24 PERp3 GND PETp2 26 GND 29 GND 29 GND 20 20 </td <td>7</td> <td></td> <td></td> <td>TDO</td> <td></td>	7			TDO	
10 +3,3V Standby +3,3 PWR 11 WAKE# Wake up PERST# Reset 12 NC GND Image: Standby Image: Standby Reset 12 NC GND REFCLK Ref clock + 14 PERp0 REFCLK Ref clock - 15 PERn0 GND Image: Standby 16 GND PETp0 Image: Standby Image: Standby 17 PRSNT2# PETn0 Image: Standby Image: Standby 18 GND GND GND Image: Standby Image: Standby 20 PERp1 MC GND Image: Standby Image: Standby Image: Standby 21 GND PETp1 GND Image: Standby Image: Standby<	8	+3,3V	PWR	TMS	JTAG -NC
Image: Note of the section of the sectin of the sectin of the section of the section of the section of	9	TRST#	JTAG - NC	+3,3	PWR
12 NC GND 13 GND REFCLK Ref clock + 14 PERp0 GND REFCLK Ref clock - 15 PERn0 GND GND Image: Strength strenght strength strenght strength	10	+3,3V	Standby	+3,3	PWR
13 GND REFCLK Ref clock + 14 PERp0 GND REFCLK Ref clock - 15 PERn0 GND GND 16 GND PETp0 Interpo 17 PRSNT2# PETn0 18 GND GND Interpo 19 PERp1 NC 20 PERn1 GND Interpo 21 GND PETp1 Interpo 22 GND PETp1 Interpo 23 PERp2 GND Interpo 24 PERp2 GND Interpo 25 GND PETp2 Interpo 26 GND PETp2 Interpo 27 PERp3 GND Interpo 28 PERn3 GND Interpo 30 NC PETp3 Interpo 31 PRSNT2# GND Interpo 32 GND NC Interpo 33 PERp4 NC Interpo 34 PERp5 <		WAKE#			Reset
14 PERp0 REFCLK- Ref clock - 15 PERn0 GND GND 16 GND PETp0 17 PRSNT2# PETn0 18 GND GND 19 PERp1 NC 20 PERn1 GND 21 GND PETp1 22 GND PETp1 23 PERp2 GND 24 PERp2 GND 25 GND PETp2 26 GND PETp2 26 GND PETp3 30 NC PETp3 30 NC PETp3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 35 GND PETp4 <			NC		
15 PERn0 GND 16 GND PETp0 17 PRSNT2# PETn0 18 GND GND 19 PERp1 NC 20 PERn1 GND 21 GND PETp1 22 GND PETp1 23 PERp2 GND 24 PERp2 GND 25 GND PETp2 26 GND PETp2 27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETp5 38 PERn5 GND 39 GND PETp5 40 GND PETp5 40 GND PETp5 40 <	13	GND			
16 GND PETp0 17 PRSNT2# PETn0 18 GND GND 19 PERp1 NC 20 PERn1 GND 21 GND PETp1 22 GND PETp1 23 PERp2 GND 24 PERp2 GND 25 GND PETp2 26 GND PETp2 26 GND PETp3 30 NC PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETp5 38 PERn5 GND 39 GND PETp5 40 GND PETp5 40 GND PETn5 41 PERp6					Ref clock -
17 PRSNT2# PETn0 18 GND GND 19 PERp1 NC 20 PERn1 GND 21 GND PETp1 22 GND PETp1 23 PERp2 GND 24 PERp2 GND 25 GND PETp2 26 GND PETp2 26 GND PETp2 26 GND PETp3 30 PERp3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETp5 39 GND PETp5 40 GND PETp5 40 GND PETp5 41 PERp6 GND 42 PERn6 GND	15	PERn0		GND	
18 GND GND 19 PERp1 NC 20 PERn1 GND 21 GND PETp1 22 GND PETp1 23 PERp2 GND 24 PERp2 GND 25 GND PETp2 26 GND PETp2 26 GND PETp2 26 GND PETp2 27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETp5 40 GND PETp5 40 GND PETp5 40 GND PETn5 41 PERp6	16				
19 PERp1 NC 20 PERn1 GND GND 21 GND PETp1 22 21 GND PETp1 22 22 GND PETp1 22 23 PERp2 GND 24 24 PERp2 GND 25 26 GND PETp2 26 27 PERp3 GND 28 28 PERn3 GND 29 30 NC PETp3 30 31 PRSNT2# GND NC 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND 38 35 GND PETp4 36 GND 33 38 PERn5 GND 33 S S 39 GND PETp5 40 GND 41 41 PERp6 GND 42 PERn6<					
20 PERn1 GND 21 GND PETp1 22 GND PETp1 23 PERp2 GND 24 PERp2 GND 25 GND PETp2 26 GND PETp2 26 GND PETn2 27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETp4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETp5 41 PERp6 GND 42 PERn6 GND				GND	
21 GND PETp1 22 GND PETn1 23 PERp2 GND 24 PERn2 GND 25 GND PETp2 26 GND PETn2 27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETp4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETp5 41 PERp6 GND 42 PERn6 GND					NC
22 GND PETn1 23 PERp2 GND 24 PERn2 GND 25 GND PETp2 26 GND PETn2 27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETp4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	20	PERn1			
23 PERp2 GND 24 PERn2 GND 25 GND PETp2 26 GND PETn2 27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 34 PERn4 GND 35 GND PETp4 36 GND PETp4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	21	GND		PETp1	
24 PERn2 GND 25 GND PETp2 26 GND PETn2 27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 35 GND PETp4 36 GND PETp4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETp5 41 PERp6 GND 42 PERn6 GND	22	GND		PETn1	
25 GND PETp2 26 GND PETn2 27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 34 PERn4 GND 35 GND PETp4 36 GND PETn4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND		PERp2		GND	
26 GND PETn2 27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETp4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND		PERn2			
27 PERp3 GND 28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETn4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND					
28 PERn3 GND 29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETn4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	26			PETn2	
29 GND PETp3 30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETn4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	27				
30 NC PETn3 31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETn4 37 PERp5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	28	PERn3		GND	
31 PRSNT2# GND 32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETn4 37 PERp5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	29	GND			
32 GND NC 33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETn4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	30		NC	PETn3	
33 PERp4 NC 34 PERn4 GND 35 GND PETp4 36 GND PETn4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND				GND	
34 PERn4 GND 35 GND PETp4 36 GND PETn4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND					
35 GND PETp4 36 GND PETn4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND					NC
36 GND PETn4 37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	34	PERn4		GND	
37 PERp5 GND 38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	35	GND		PETp4	
38 PERn5 GND 39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	36	GND			
39 GND PETp5 40 GND PETn5 41 PERp6 GND 42 PERn6 GND	37	•			
40 GND PETn5 41 PERp6 GND 42 PERn6 GND	38	PERn5		GND	
41 PERp6 GND 42 PERn6 GND	39	GND		PETp5	
42 PERn6 GND	40	GND		PETn5	
	41	PERp6		GND	
43 GND PETp6	42	PERn6		GND	
	43	GND		PETp6	

Pi	Side B	Descriptio	Side A	Descriptio
44	GND		PETn6	
45	PERp7		GND	
46	PERn7		GND	
47	GND		PETp7	
48	PRSSNT2		PETn7	
49	GND		GND	
50	PERp8		NC	
51	PERn8		GND	
52	GND		PETp8	
53	GND		PETn8	
54	PERp9		GND	
55	PERn9		GND	
56	GND		PETp9	
57	GND		PETn9	
58	PERp10		GND	
59	PERn10		GND	
60	GND		PETp10	
61	GND		PETn10	
62	PERp11		GND	
63	PERn11		GND	
64	GND		PETp11	
65	GND		PETn11	
66	PERp12		GND	
67	PERn12		GND	
68	GND		PETp12	
69	GND		PETn12	
70	PERp13		GND	
71	PERn13		GND	
72	GND		PETp13	
73	GND		PETn13	
74	PERp14		GND	
75	PERn14		GND	
76	GND		PETp14	
77	GND		PETn14	
78	PERp15		GND	
79	PERn15		GND	
80	GND		PETp15	
81	PRSNT2#		PETn15	
82		NC	GND	

Table 12: PCIe Edge Connector Pin-Out

Compliance and Regulatory Testing

EMC Compliance

The Dolphin PCI Express PXH832 adapter has been tested to the following relevant test standards for PCI Express cards, telecommunication and industry equipment installed in a standard PC:

EN 55022 (2010), Class B EN 55024 (2010), Class A EN 61000-6-2 (2005)

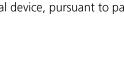
This does not ensure that it will comply with these standards in any random PC. It is the responsibility of the integrator to ensure that their products are compliant with all regulations where their product will be used.

RoHS Compliance

The Dolphin PXH832 is RoHS compliant. A Compliance certificate issued by the manufacturer is available upon request.

FCC Class A

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules.







Limited Warranty

Dolphin Interconnect Solutions warrants this product to be free from manufacturing defects under the following terms:

Warranty Period

The warranty applies for one (1) year from the date of purchase. Extended warranty is available.

Coverage

To the extent permitted by applicable law, this warranty does not apply to:

- Damage caused by operator error or non-compliance with instructions available for the product.
- Use or attempt to use or program firmware not approved by Dolphin.
- Damage due to accidents, abuse, misuse, improper handling or installation, moisture, corrosive environments, high voltage surges, shipping, or abnormal working conditions.
- Damage caused by acts of nature, e.g. floods, storms, fire, or earthquakes.
- Damage caused by any power source out of range or not provided with the product.
- Normal wear and tear.
- Attempts to repair, modify, open, or upgrade the product by personnel or agents not authorized by Dolphin.
- Products for which the serial number label has been tampered with or removed.
- Damage to the product caused by products not supplied by Dolphin.

Service Procedure

In the event that the product proves defective during the Warranty Period, you should contact the seller that supplied you with the product, or if you purchased it directly from Dolphin, visit <u>https://www.dolphinics.com/csp</u> to obtain a valid RMA number and instructions. Products returned to Dolphin without a proper RMA number will not be serviced under this warranty.