SGPCI64

User Guide

Revision Information: Revision 1.0

Hardware Version: SGPCI64-A0

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Preface

This manual describes how to use the SGPCI64 board for the purpose of StarFabric system development and evaluation of the SG2010 PCI-to-StarFabric device.

Audience

This manual is written for users of the SGPCI64 board.

Overview

This manual contains the following chapters and appendices, and a glossary:

Chapter 1 Introduction – Overview of the SGPCI64 board

Chapter 2 Feature Summary – Describes main features of the product

Chapter 3 Operation and Installation – Describes typical installation and configuration of the product

Chapter 4 Debug and Observation Points – Describes convenient access points for signal observation

Appendix A Bill of Materials – Defines list of components on PCB assembly

References and Additional Information

If you need additional information, please contact StarGen at support@stargen.com or refer to one or more of the following reference documents:

PCI Special Interest Group (PCISIG) Specifications

PCI Local Bus Specification, Revision 2.2

PCI-to-PCI Bridge Architecture Specification, Rev 1.1

PCI Industrial Computer Manufacturers Group (PICMG) Specifications

PICMG 2.0 D3.0, CompactPCI Specification

PICMG 2.1 R1.0, CompactPCI Hot Swap Specification

PICMG 2.17 StarFabric Specification

StarGen Specifications

SG2010 Hardware Reference Manual

SG2010 Data Sheet

StarFabric Architecture Specification

Fabric Programmer's Manual

SGPCI64 Schematics (Can be found on the StarGen Secure Website???????)

Revision History

Revision Number	Date mm/dd/yy	Description
1.0	**04/12/04**	Initial Revision

1 Feature Summary

2.1 Main Features

The SG2010 evaluation board has the following features:

- SG2010 PCI-to-StarFabric bridge device
- PCI Rev. 2.2 compliant interface; 64bit, 66Mhz capable
- Two (2) 2.5Gbps full-duplex StarFabric serial links available through standard RJ45 connectors
- Eight (8) LVDS serial link status LEDs
- Register configuration pre-load serial ROM
- Configuration DIP switches and jumpers

2.2 SGPCI64

Figure 2–1 SGPCI64 Front Panel

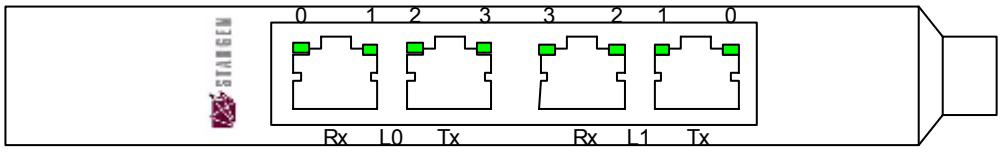
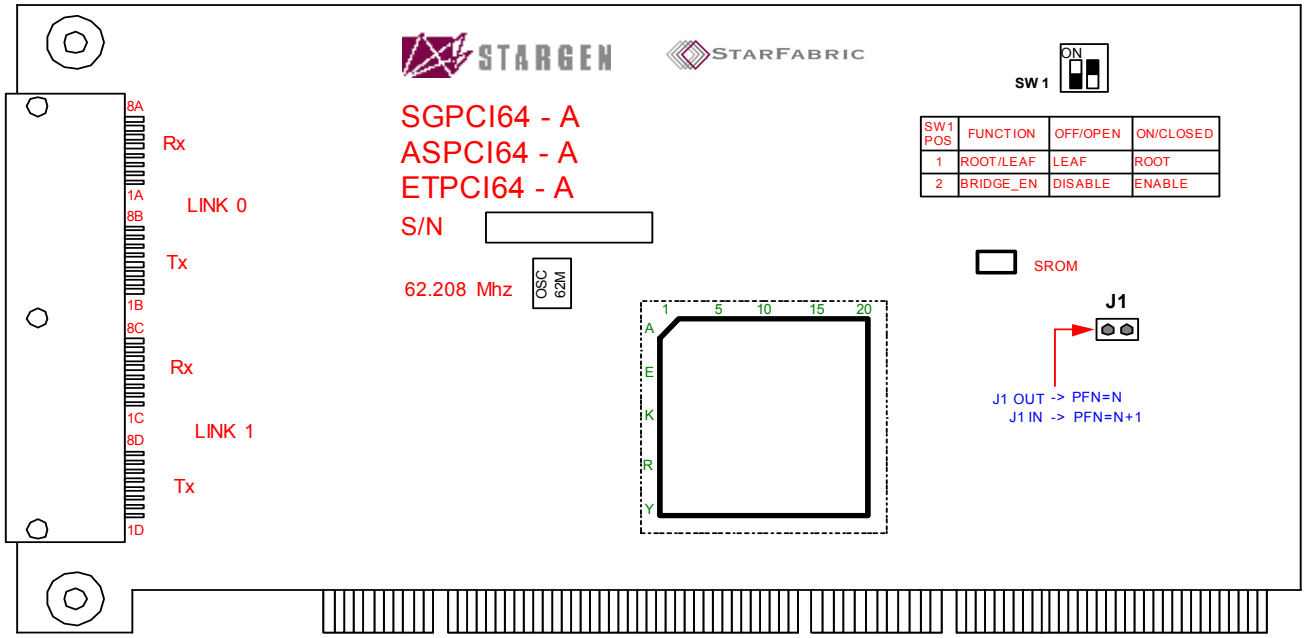


Figure 2–2 SGPCI64 PCB



2.3 DIP Switch

The SGPCI64 contains one 2 position DIP switch, SW1, that is used to configure the SG2010. The DIP switch is shown in Figure 2–2.

SW1 position 1 is used to configure the SG2010 as either a root or leaf device. Position 2 enables or disables the SG2010 PCI bridge function. Refer to the SG2010 Hardware Reference Manual for more information on the SG2010 Root and Bridge_En strapping pins.

Table 2–1 Switch (SW1) Settings

Switch	Off	On
S1	Root set logic “0”. The SG2010 is configured as a leaf device.	Root set to logic “1”. The SG2010 is configured as a root device which makes it responsible for starting Star-fabric enumeration.
S2	BRIDGE_EN set logic “0”. The SG2010’s PCI bridge function is disabled and the SG2010 cannot generate or receive address routed frames.	BRIDGE_EN set to logic “1”. The SG2010’s PCI bridge function is enabled and the SG2010 generates and receives address routed frames.

A short description of these dipswitch settings can be found below SW1 on the printed circuit board.

2.4 Reset Strapping Options

A combination of fixed resistors and the stake pin jumper J1 is used to set the configuration of the SGPCI64 at power up as indicated Table 2–2

Table 2–2 Strapping Pins

Name	Default	Alternate
PFNo	J1 jumper uninstalled In root mode FID is set to 0/0/7777777. (N)	J1 jumper installed In root mode FID is set to 1/0/7777777. (N+1)
LEDHM15	R38 installed and R35 uninstalled Differential pair state us driven on LEDx[3:0] for all 4 differential pairs within the receive link. (All LEDs)	R35 installed and R38 uninstalled Link state is driven on LEDx[0] only for each link. (One LED)

Default settings should work for most applications.

2.5 Status LEDs

The SGPCI64 has 8 status LEDs that are used to indicate the state of the LVDS receivers on both links. These LEDs are located on the front panel of the card and are grouped in two banks of four. Each group of four corresponds to the four LVDS receiver pairs in Link 0 and Link 1 of the SG2010.

Link status can be displayed in either of two modes set by the installation of R35 or R38 as shown in Table 2–2. The available operating modes are described as follows:

1. One LED providing status for each LVDS receiver differential pair.
2. One LED providing receiver status for each Starfabric “link” consisting of up to four synchronized differential pairs. The mode is selected at reset by sampling the state of the LEDHM15 pin.

The LEDs indicate the state of the associated link as shown in Table 2–3.

Table 2–3 LED States

LED State	Description
Off	Link is unsynchronized and traffic is disabled.
On	Link is synchronized and traffic is enabled.
Flashing	Link is synchronized but traffic is disabled.

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Operation and Installation

3.1 Hardware Requirements

A PC that supports PCI-to-PCI bridges is required. Most PC's manufactured within the past several years support these bridges. The PCI slots must also supply 3.3V to the PCI connectors. This is a PCI 2.2 Specification requirement.

3.2 Software Requirements

3.2.1 Use of the SG2010 PCI to PCI Bridge Function

None required.

3.2.2 Advanced Use (Path & Multicast routing)

Use StarGen Software Development Kit (SDK).

3.3 SG2010 - PCI64 Installation Procedure

1. Shutdown power to the computer
2. Confirm that the SGPCI64 DIP switch and strapping pin options are set. SGPCI64 default settings are outlined in Section 2.4.
3. Insert the SG2010-PCI64 into an available PCI slot.
4. Connect the LVDS links to their link partners via the RJ45 connector(s). Check that a link's transmitter (Tx) is connected to its partner's receiver (Rx) and vice-versa.
5. Power up the PC. If the SG2010PCI64 card is configured as a fabric root node then it should be powered up last.

3.4 Factory Default Configuration - Leaf, Gateway Only Mode

The factory default operating mode for the SGPCI64 board is Leaf and “Gateway Only” mode. This mode disables address routing support and places the device into a path route only mode of operation. This mode is generally used to interconnect two or more PC’s for distributed computing or clustering applications. The SG2010 Gateway-only mode provides address isolation for the CPU domain on its PCI interface. In distributed computing and clustering applications the Root is typically established in software, pseudo-root. Please refer to the Fabric Programmer’s Manual for more information.

3.4.1 Requirements

- SGPCI64 installed into PCI peripheral slot in a standard PC
- SG2010 bridge function disabled
- Mode set to "Leaf"

3.4.2 DIP Switch Settings

Table 3–1 Leaf/Gateway-Only Switch Positions

SW1	
S#	**Position**
1	OFF
2	OFF

3.4.3 Installation Procedure

1. Set the DIP switches, jumper settings and resistor positions as needed. Refer to Section 2.4 and Section 3.4.2 for more detail.
2. Install the SGPCI64 board into any PCI peripheral slot
3. Connect the LVDS links to their link partners via the dual RJ45 connector(s)
4. Turn on PC power
5. If the board is in a multi-computing environment make sure that one of the “leaf” devices is setup as a pseudo-root. Initial diagnosis in a Win98 or DOS environment, can be done with the "sroot" command in the StarGen-supplied pvx utility. Also, the StarFabric bus drivers provided by StarGen can be used to execute pseudo-root automatically. Please see StarGen’s software development kit for more details on pseudo-root

3.5 PCI Bridge Mode Configuration

The SGPCI64 board can also be setup to enable legacy PCI support for PCI Expansion applications. In these applications the SG2010 should be setup as a Root with its Bridge function enabled. This mode also allows for a mixed mode, both address routed and path-routed traffic.

3.5.1 Requirements

- SGPCI64 installed into PCI peripheral slot in a standard PC
- SG2010 bridge function enabled
- Set to the board to either “root” mode.

3.5.2 DIP Switch Settings

Table 3–2 Root/Bridge Enabled Switch Positions

SW1	
S#	**Position**
1	ON
2	ON

3.5.3 Installation Procedure

1. Set the DIP switches, jumper settings and resistor positions as needed. Refer to Section 2.4 and Section 3.5.2 for more detail.
2. Install the SGPCI64 board into any PCI peripheral slot
3. Connect the LVDS links to their link partners via the dual RJ45 connector(s)
3 Turn on all other StarFabric devices. The Root of the Fabric should be powered last.
4 Turn on PC power.

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Appendix A

Bill of Materials

Materials List (Refer to Appendix B for Related Schematics)

DNI = Do Not Install

#	QTY	REFDES	VENDOR	VENDOR PN	PACKAGE	VALUE	PART_SPEC	COMMENT
1	1	P1			94P_D		64-BIT PCI EDGE FINGERS	
2	2	U1,U8			MTHOLE1		BRACKET MOUNTING HOLE	
3	1	J2	AMPHENOL	RJSS538104	32PRJ45		4-PORT RJ45 CONNECTOR W/LIGHT	
4	8	C11,C89, C94-99	ANY	TO PART_SPEC	C0603	.022UF	X7R SMT 16V 10%	
5	1	C4	ANY	TO PART_SPEC	RLP-182	10UF	TANTALUM 10UF 16V	
6	1	C46	ANY	TO PART_SPEC	C0402	.068UF	Y5V SMT 16V 20%	
7	1	C100	ANY	TO PART_SPEC	C0603	.22UF	X7R SMT 16V 10%	
8	5	C3,C5,C7-9	ANY	TO PART_SPEC	RLP-183	22UF	TANTALUM 22UF 16V	
9	27	C13-20, C29-36, C44, C48-49, C52, C62-63, C68-69, C71,C78-79	ANY	TO PART_SPEC	C0402	.001UF	X7R SMT 16V 10%	
10	35	C21-28, C38-43, C47,C50, C53-57, C59,C61, C66-67, C70,C74, C76-77, C82-83,	ANY	TO PART_SPEC	C0402	.01UF	X7R SMT 16V 10%	

		C88,C91-93						
11	2	R8,R12	ANY	TO PART_SPEC	R0402	20K	SMT 1% 0.0625W	
12	2	R22,R32	ANY	TO PART_SPEC	R0402	100	SMT 1% 0.0625W	
13	3	R11,R14,	ANY	TO PART_SPEC	R0402	0	SMT 1% 0.0625W	
		R57						
14	1	R13	ANY	TO PART_SPEC	R0402	0	SMT 1% 0.0625W	DNI
15	24	C1-2,C6,	ANY	TO PART_SPEC	C0603	.1UF	X7R SMT 16V 10%	
		C10,C12,						
		C37,C45,						
		C51,C58,						
		C60,						
		C64-65,						
		C72-73,						
		C75,						
		C80-81,						
		C84-87,						
		C90,						
		C101-102						
16	2	R25,R27	ANY	TO PART_SPEC	R0402	1.75K	SMT 1% 0.0625W	
17	1	R58	ANY	TO PART_SPEC	R0402	4.99K	SMT 5% 0.1W	DNI
18	8	R1-3,R5,	ANY	TO PART_SPEC	R0402	120	SMT 5% 0.0625W	
		R7,R9-10,						
		R15						
19	30	R4,R6,	ANY	TO PART_SPEC	R0402	10K	SMT 1% 0.0625W	
		R16-17,						
		R28-31,						
		R33-34,						
		R36,R38-56						
20	1	R23	ANY	TO PART_SPEC	R0402	6.2	SMT 5% 0.0625W	DNI
21	1	R37	ANY	TO PART_SPEC	R0402	43	SMT 1% 0.0625W	
22	1	R35	ANY	TO PART_SPEC	R0402	1K	SMT 1% 0.0625W	DNI
23	4	R18-19,	ANY	TO PART_SPEC	R0402	1K	SMT 1% 0.0625W	
		R24,R26						
24	1	R20	ANY	TO PART_SPEC	R0402	191	SMT 1% 0.0625W	
25	1	R21	ANY	TO PART_SPEC	R0402	40	SMT 1% 0.0625W	
26	1	U2	ATMEL	AT25640N-10SC-2.7	8PSOIC		64K SERIAL ROM	
			ATMEL	AT25640AN-10SI-2.7				
27	1	SW1	C&K COMPON	SD02HOSK	4PDIP		2 POSITION DIPSWITCH SMT	
28	2	L2,L5	COILCRAFT	D01608C-222	DS1608C	2.2UH	15UH POWER INDUCTOR	
29	1	L3	COILCRAFT	0805CS-821X_BC	0805CS	820NH		
30	4	L1,L4,L6,	COILCRAFT	0603CS-R12X_BC	0603CS	120NH		

		L10						
31	1	XS1	IRONWOOD E SG-BGA-6010		X272PBGA		SOCKET FOR 272BGA	DNI
32	1	U7	LINEAR TEC LT1963AEST-1.5		SOT223		LDO 1.5V 1.5A REGULATOR	
33	8	DS1-8	LITEON	LTST-C170GKT	SMT_0805	GRN	SMT GREEN LED	
34	8	L7-9,	MURATA	DLW21HN900SQ2L	CM3_2X1_6		HIGH FREQ COMMON MODE CHOKES	
		L11-15						
35	2	U4-5	ON	MC74LCX74DT	TSSOP14		DUAL D FLIP FLOP	
36	1	U3	PHILIPS	74LVC1G14GW-G	SOT353		SINGLE SCMITT-TRIGGER INVERTER	
			TI	SN74LVC1G14DCK				
37	1	U6	STARGEN	SG2010	SG3010-B		STARFABRIC TO PCI BRIDGE	
38	1	OSC1	TRANSKO	TSM30DJR62.208M	5X7SMD	62.208MHZ	62.208 MHZ OSC 20PPM	
			CARDINAL C	CPPFXC7L-BD-62.208PD				
39	1	J1	TYCO	644695-2	CAMP644695		SINGLE ROW 2 PIN .1 HEADER	DNI

Glossary

DIP	Dual in line package
GPIO Signals	General Purpose I/O Signals
PCI	Peripheral Component Interconnect
SROM	Serial Read-Only Memory